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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,879	10/11/2004	Jui-Yuan Chou	13453-US-PA	5878

31561 7590 05/22/2007

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PATEL, NITIN	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
05/22/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/711,879	CHOU ET AL.	
	Examiner	Art Unit	
	Nitin Patel	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-20* is/are allowed.

6)☒ Claim(s) *1,2,4-9 and 11-14* is/are rejected.

7)☒ Claim(s) *15-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,4-9,11-14 rejected under 35 U.S.C. 102(b) as being anticipated by Ha (6,493,047).

As per claims 1,8 Ha shows a thin film transistor array plate, comprising: a substrate, having a display region and a peripheral circuit region; a plurality of pixel structures, disposed inside the display region; a plurality of switching devices, disposed inside the peripheral circuit region (in fig.3 elements 40,42 and pixel region at the intersection of G1 and D1); a plurality of lead lines, disposed on the substrate, wherein each one of the lead lines electrically connects to the corresponding pixel structures and one of the switching devices; and a plurality of electrostatic discharge (ESD) protection circuits(in fig. 3A-3D and in col.3-4 lines 65-30), disposed inside the peripheral circuit region, wherein each one of the ESD protection circuits is electrically connected to the corresponding switching devices(In fig.3).

As per claims 2,9 Ha shows the lead lines comprise a plurality of gate lines and a plurality of source lines (In fig.3 elements G1...GN and D1...DM).

As per claims 4,11 Ha also teach wherein the switching devices comprise thin film transistors (in fig.3 element 40).

As per claims 5-7,12-14 Ha shows each switching device comprises at least two serially connected thin film transistors (in fig.3c) and wherein each switching device comprises at least two parallel-connected thin film transistors (in fig.4 element PR2 is parallel transistors) and switching device plurality of parallel and serially connected (in fig.4 both PR1 and PR2 is connected to element 58 and both are individually is serial and parallel switching elements).

Allowable Subject Matter

2. Claims 3,10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art fails to teach or suggest the ESD protection circuits comprises: a first electrostatic discharge protection circuit, electrically connected to odd numbered gate lines; a second electrostatic discharge protection circuit, electrically connected to even numbered gate lines; a third electrostatic discharge protection circuit electrically connected to odd numbered source lines; and a fourth electrostatic discharge protection circuit, electrically connected to even numbered source lines as claimed in claims 3,10.

3. Claims 15-20 are allowed.

The prior art fails to teach or suggest A thin film transistor array plate, comprising: a substrate, having a display region and a peripheral circuit region; a plurality of gate lines, disposed on the substrate; a plurality of source lines, disposed on the substrate, wherein the gate lines and the source lines define the display region into a plurality of pixel areas; a plurality of thin film transistor, each thin film transistor

disposed inside one of the pixel area, wherein each one of the thin film transistors is electrically connected to one of the gate lines and one of the source lines correspondingly; a plurality of pixel electrode, each pixel electrode positioned inside one of the pixel areas and electrically connected to a corresponding thin film transistor; a plurality of switching devices, disposed inside the peripheral circuit region, wherein each one of the switching devices is electrically connected to one of the gate lines and the source lines; a first electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the first electrostatic discharge protection circuit is electrically connected to odd numbered gate lines through portions of the switching devices; a second electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the second electrostatic discharge protection circuit is electrically connected to even numbered gate lines through portions of the switching devices; a third electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the third electrostatic discharge protection circuit is electrically connected to odd numbered source lines through portions of the switching devices; and a fourth electrostatic discharge protection circuit, disposed inside the peripheral circuit region, wherein the fourth electrostatic discharge protection circuit is electrically connected to even numbered source lines through portions of the switching devices as claimed in claim 15.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin Patel
Primary Examiner
Art Unit 2629

NP

NITIN I. PATEL
PRIMARY EXAMINER